AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

What is claimed is:

1. (currently amended): A semiconductor memory device comprising:

a memory; and

a memory control circuit for controlling said memory, wherein [[:]] said memory control circuit ~~includes~~ comprises:

a bank busy circuit for variably setting a bank busy time that controls different bank cycle times;

a read data input circuit having variable input timing for inputting read data output from said memory ~~in variable input timing~~;

a write data output circuit having variable output timing for outputting write data to said memory ~~in variable output timing~~;

a command control circuit for issuing a command to said memory based on a memory command output from said bank busy circuit ~~thereby controlling different command interfaces~~;

a write mask circuit for controlling different write masks;

an initial sequence control circuit for controlling memories having different ~~in the~~ initial ~~sequence~~ sequences; and

an address generation circuit for controlling different address interfaces ~~, and~~

~~said memory control circuit controls different memories using the same hardware~~.

2. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said bank busy circuit ~~includes~~ comprises:

a program register for variably setting the bank busy time; and

a bank busy counter for setting a value ~~set~~ on said program register~~,~~ and ~~then~~ counting down the set value for each clock cycle when a bank [[n]] is accessed ~~for turning on~~, ~~and~~ wherein

said bank busy circuit provides said command control circuit with a memory command indicating cleared bank busy when ~~the logic~~ said set value of said bank busy counter becomes zero ~~, thereby controlling memories different in the bank cycle time~~.

3. (currently amended): The semiconductor memory device according to claim 1, wherein:

said read data input circuit ~~includes~~ comprises a first program register for variably setting the input timing of the read data output from said memory ~~for controlling memories different in the access time,~~ and ~~inputs~~ inputting the read data output from said memory based on a variable input timing ~~set~~ value set in ~~on~~ the first program register ~~in variable input timing~~, and

said write data output circuit comprises a second program register for variably setting the output timing of the write data output to said memory [[,]] and ~~adjusts~~ adjusting the write data output timing based on a ~~set vale~~ value set in ~~on~~ the second program register.

4. (original): The semiconductor memory device according to claim 1, wherein said bank busy circuit switches the bank busy time using a switch.

5. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said write mask circuit ~~relates to mask control for the write data output to said memory, and has~~ comprises a program register for switching between masking a write operation using a Variable Write function when an FCRAM or an NWRAM is used, and masking the write operation using a Data Mask function when a DDR-SDRAM is used.

6. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said write mask circuit ~~relates to mask control for the write data output to said memory, and has~~ comprises a switch for switching between masking ~~of~~ a write operation using a Variable Write function when an FCRAM or an NWRAM is used, and masking ~~of~~ the write operation using a Data Mask function when a DDR-SDRAM is used.

7. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said address generation circuit ~~relates to address generation of memories different in address assignment, and includes~~ comprises a program register for switching address generation logic.

8. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said address generation circuit ~~relates to address generation of memories different in address assignment, and includes~~ comprises a switch for switching address generation logic.

9. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said initial sequence control circuit ~~relates to control of memories different in the initial sequence, includes~~ comprises a program register for variably changing the issue sequence of commands ~~including~~ comprising mode register set, extension mode register set, auto refresh, and all bank pre-charge, and for variably changing set values on a mode register and an extension mode register, ~~controls said memories different in the initial sequence using the same circuit,~~ and for ~~issues~~ issuing an initial sequence command ~~including~~ comprising the mode register set, the extension mode register set, the auto refresh, and the all bank pre-charge to said command control circuit.

10. (currently amended): The semiconductor memory device according to claim 1, wherein [[:]] said initial sequence control circuit ~~relates to control of memories having different~~

~~initial sequences, includes~~ comprises a switch for variably changing the issue sequence of commands ~~including~~ comprising mode register set, extension mode register set, auto refresh, and all bank pre-charge, and for variably changing set values on a mode register and an extension mode register, ~~controls said memories different in the initial sequence using the same circuit,~~ and for ~~issues~~ issuing an initial sequence command ~~including~~ comprising the mode register set, the extension mode register set, the auto refresh, and the all bank pre-charge to said command control circuit.

11. (original): The semiconductor memory device according to claim 1, comprising a power supply capable of adjusting a power supply output level supplied for said memory.

12. (currently amended): A mount-type semiconductor device for mounting said semiconductor memory device according to claim 1, ~~on~~ comprising a circuit board for interconnecting a plurality of different memory devices, each memory device having different package sizes or pin assignments to a motherboard, wherein [[:]] said interconnection between the motherboard and the circuit board has only one physical configuration ~~said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted~~.

13. (currently amended): A mount-type semiconductor device for mounting said semiconductor memory device according to claim 2, ~~on~~ comprising a circuit board for interconnecting a plurality of different memory devices, each memory device having different package sizes or pin assignments to a motherboard, wherein [[:]] said interconnection between the motherboard and the circuit board has only one physical configuration ~~said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted~~.

14. (currently amended): A mount-type semiconductor device for mounting said semiconductor memory device according to claim 3, comprising ~~on~~ a circuit board for interconnecting a plurality of different memory devices, each memory device having different package sizes or pin assignments to a motherboard, wherein [[:]] said interconnection between the motherboard and the circuit board has only one physical configuration ~~said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted~~.

15. (original): The mount-type semiconductor device according to claim 12, wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

16. (original): The mount-type semiconductor device according to claim 13, wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

17. (original): The mount-type semiconductor device according to claim 14, wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

18. (currently amended): A mount-type semiconductor device for mounting said semiconductor memory device according to claim 1 on a circuit board for interconnecting said memory device to a motherboard, wherein:

said circuit board comprises a DIMM (Dual Inline Memory Module), and a terminating resistor where said memory device does not comprise a terminating resistor; and

said interconnection between the motherboard and the DIMM has only one physical configuration.

~~said memory is different in whether a terminating resistor is incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted, a terminating resistor is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a terminating resistor is attached to a~~

~~DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.~~

19. (currently amended): A mount-type semiconductor device for mounting said semiconductor memory device according to claim 2 on a circuit board for interconnecting said memory device to a motherboard, wherein:

said circuit board comprises a DIMM (Dual Inline Memory Module), and ~~said memory is different in whether~~ a terminating resistor where said memory device does not comprise ~~is incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted,~~ a terminating resistor; and

said interconnection between the motherboard and the DIMM has only one physical configuration. ~~is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a terminating resistor is attached to a DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.~~

20. (currently amended): A mount-type semiconductor device for mounting said semiconductor memory device according to claim 3 on a circuit board for interconnecting said memory device to a motherboard, wherein:

said circuit board comprises a DIMM (Dual Inline Memory Module), and ~~said memory is different in whether~~ a terminating resistor where said memory device does not comprise ~~is~~

~~incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted,~~ a terminating resistor; and

said interconnection between the motherboard and the DIMM has only one physical configuration. ~~is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a terminating resistor is attached to a DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.~~